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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,525	07/08/2003	Tsuneo Hamaguchi	009683-472	9010

7590 08/25/2004  
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EXAMINER

DOLAN, JENNIFER M

ART UNIT	PAPER NUMBER
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2813

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/614,525

Applicant(s)

HAMAGUCHI ET AL.

Examiner

Jennifer M. Dolan

Art Unit

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 12-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 12-15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. ____.  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>7/8/03</u> .  | 6) <input type="checkbox"/> Other: ____.                                    |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The applicant claims that the linear expansion coefficient of the electronic component is smaller than that of "a wiring substrate." Since the method and/or device as claimed does not include a wiring substrate, and since a generic or unspecified wiring substrate could be made of any number of materials with vastly differing thermal expansion coefficients, it is not clear exactly what is being claimed: i.e., whether the electronic component simply has a smaller coefficient than some common or generic wiring substrate material, or whether the wiring substrate refers to either the semiconductor device substrate or the mounting board substrate. For the purposes of examination, it is assumed that "a wiring substrate" is the same thing as the semiconductor device substrate, in order to conform to the written description of the invention.

*Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,437,990 to Degani et al. (cited by applicant) in view of Japanese Patent Publication No. 2000-031316 to Ishibashi (cited by applicant).

Regarding claim 12, Degani discloses a method for manufacturing an electronic equipment by: mounting a semiconductor device (22, 21, 31-34) on a mounting board (26) with projecting electrodes (27) interposed therebetween (figure 2), the device having the projecting electrodes and a chip (33) provided on a mounting side thereof (figure 2), and having an electronic component (21) provided on a side opposite to the mounting side (figure 2), wherein the chip has a thickness smaller than a height of the projecting electrodes (figure 2), the component has a thickness larger than that of the chip (figure 2; column 1, lines 60-67; column 3, lines 1-20), and the device is mounted on the mounting board with the projecting electrodes interposed therebetween (figure 2) by aligning the mounting board with the device and pressing the device on the mounting board (column 3, line 10 – column 4, line 30).

Degani fails to suggest that the device is warped so as to be recessed on the mounting side.

Ishibashi teaches warping a device so as to be recessed on the mounting side (figures 1 and 4). Ishibashi further shows that it is possible to have chips attached to either a concave side or a convex side of the warped device substrate (see figures 1, 4, 5, and 10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device substrate of Degani, such that is attached to the mounting board in a warped state, as suggested by Ishibashi. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide the device substrate warped so as to be recessed on the mounting side, because Ishibashi shows that warping of a substrate is expected due to differences in thermal expansion between the various components of the assembly (see Ishibashi, paragraph 0003), which in turn, can lead to poor solder ball connections (Ishibashi, paragraph 0004). By attaching the substrate to the mounting board in an already warped position in the manner suggested by Ishibashi, however, it is possible to control the vertical position of the solder joints as well as the overall position of the chip, such that low cost, highly stable solder joints between a device and a mother board can be formed (see Ishibashi, paragraphs 0013, 0016, 0017, 0031).

Regarding claim 15, all of the process steps must be intrinsically be present in the combination of Degani et al. and Ishibashi. Degani teaches the steps of bonding the component to a wiring substrate as specified (see column 2, lines 25-40, column 3, lines 20-30, column 4, lines 15-40; die bonding processes require heating steps followed by cooling)., mounting the chip on the mounting side (column 4, lines 15-20) and forming the projecting electrodes on the mounting side (column 1, lines 30-35). Ishibashi shows that by mounting a component on the top side of a wiring substrate, the substrate will curve based on thermal expansion (see Ishibashi,

Art Unit: 2813

paragraph 0003-0005). Since the combination of Degani and Ishibashi applied supra to claim 12 includes using the device of Degani, but applying and accommodating a device warpage, as taught by Ishibashi, the combination must include all of the claimed steps.

5. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Degani et al. in view of Ishibashi, as applied to claim 12 above, and further in view of Japanese Patent Publication 10-79405 to Hozoji et al (cited by applicant).

Degani and Ishibashi are considered to teach device package components commonly used in the art, such as silicon chips or resinous wiring substrates. Ishibashi further teaches that the device substrate curves based on the difference in the thermal expansion coefficients between the chip and the wiring substrate, such that the substrate curves in a direction opposite to the chip (see paragraphs 0008-0010, 0013, 0021, 0024).

Neither Degani nor Ishibashi specifically teach the composition of the device substrate or the chips.

Hozoji teaches a structure including the claimed components, and further specifies that that a typical BGA wiring substrate has a thermal expansion of 17-25 ppm/degree C, whereas a typical semiconductor chip has a thermal expansion of 3-5 ppm/degree C (see paragraph 0004; figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the electronic component of Degani as modified by Ishibashi has a smaller linear expansion coefficient than the wiring substrate, and about an equal expansion coefficient to the chips, as suggested by Hozoji. The rationale is as follows: A person having

Art Unit: 2813

ordinary skill in the art would have been motivated to specify that the electronic component and chips are both silicon or another semiconductor material, and that the wiring substrate is a resin, plastic, or metal, as is conventional and well-known in the art, thus having expansion coefficients of about 3-5 ppm/degree C, 3-5 ppm/degree C, and 17-25 ppm/degree C, respectively (see paragraph 0004; figure 1 of Hozoji). Also, a person skilled in the art would recognize that in order for the substrate of Ishibashi to curve in a manner concave downward when heat is applied, the substrate must expand at a faster rate than the chip (see figures 1 and 4 of Ishibashi).

### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- a. U.S. Patent No. 6,518,666 to Ikeda discloses bending of a wiring substrate based on relative thermal expansion coefficients of chips or encapsulants.
- b. U.S. Patent No. 6,396,159 to Shoji teaches bending of a wiring substrate due to CTE differences between a chip and an encapsulant.
- c. U.S. Patent No. 5,986,217 to Strum discloses attaching an expansion layer to a PCB in order to force a thermal warpage in order to induce rotational stresses on the solder joints between a chip and PCB, rather than linear shear.
- d. U.S. Patent No. 6,271,109 to Weygan et al. teaches altering the height of solder balls to accommodate the thermal warping of the wiring board.

Art Unit: 2813

- e. U.S. Patent No. 6,417,027 to Akram teaches the use of flexible wiring substrates to conform to non-planar wiring surfaces.
- f. PCT publication WO 97/04629 to Robinson et al. discusses methods for accommodating wiring board warpage due to CTE differences.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan  
Examiner  
Art Unit 2813

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